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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,743	04/19/2001	Gerald Deboy	GR 99 P 2591 P	9326

7590 02/26/2004

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/838,743	DEBOY ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/29/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,7,9 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7,9 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/29/03 has been entered.

Response to Amendment

Amendment filed 11/25/03 has been entered following and in view of aforementioned Request for Continued Examination. In said Amendment Applicants substantially amended claims 1, 6, 7, 9 and 10 through substantial amendment of claim 1. Applicants cancelled claims 2-5, 8 and 11-12. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. ***Claims 1, 6, 7, 9 and 10*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, the amendment of claim 1 introduces new matter

(a) because the compensation component (Figures 4 and 5 and pages has not been disclosed to have a gate insulated from the semiconductor body; instead, Figure 4 clearly shows said gate not to be insulated from said body but instead to abut the latter;

(b) because the compensation component has not been disclosed to have heavily doped terminal regions (corresponding to 9 in Figure 1 or 27 in Figure 5) disposed at the second (i.e., *lower*) main surface, i.e., the surface opposite the gate;

(c) because a further zone of first conductivity (corresponding to zone 10 in Figure 1) disposed in a vicinity of said second main surface has not been disclosed for the compensation component; and

(d) because punch-through regions (such as 12 in Figure 12) disposed between said heavily doped terminal regions have not been disclosed for the compensation component at least for lack of disclosure of said heavily doped terminal regions.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claims 1, 9 and 10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (6,051,850) in view of Chen (US 2003/0160281 A1) and Nagasu et al (6,204,717).

On claim 1, Park teaches:

a semiconductor body 100/116/104 (cf. col. 3, l. 52 – col. 4, l. 43) of first conductivity type (n-type) and having a first main surface (upper surface) and a second main surface (lower surface) opposite said main surface;

a body zone 108 (cf. col. 3, l. 52 – col. 4, l. 43) of second conductivity type (p-type) opposite said first conductivity type introduced into said first main surface;

a zone 110 (cf. col. 3, l. 52 – col. 4, l. 43) of said first conductivity type disposed in said body zone;

a first electrode 114 (cf. col. 3, l. 52 – col. 4, l. 64) making contact with said zone and body zone;

a second electrode 112 (cf. Fig. 1) disposed on said second main surface;

an insulating layer disposed on said first main surface (cf. col. 4, l. 27-43);

a gate electrode 118 (cf. col. 4, l. 43-51) disposed above said body zone and separated from said body zone by said insulating layer (cf. col. 4, l. 27-43);

an intersection of said semiconductor body and said body zone defining a pn junction (i.e., the pn junction between 104 and 108) (cf. Figure 1);

said semiconductor body having:

heavily doped terminal regions 100 (cf. col. 3, l. 52 – col. 4, l. 43) of said first conductivity type disposed at said second main surface;

a further zone 116 (cf. cf. col. 3, l. 52 – col. 4, l. 43) of said first conductivity type disposed in a vicinity of said second main surface; and

punch-through regions 102 (cf. col. 3, l. 52 – col. 4, l. 43) disposed between said heavily doped terminal regions, a current/voltage characteristic in breakdown being controlled through an area ratio between said heavily doped terminal regions and said punch-through regions.

Park does not necessarily teach the further limitations of (a) the layer thickness as claimed in lines 8-16 in page 5 of the text claim 1 in said Amendment, and (b) the compensation layer as claimed in lines 5-6 of page 5 in the text of claim 1 in said Amendment. *However, it would have been obvious to include further limitation* (a) in view of Nagasu et al, who teach, in a patent drawn to a vertical power semiconductor device (Figures 10, i.e., analogous art) that the voltage V_p (cf. col. 16, l. 29-38) at maximum width (punch-through condition) of the depletion layer 28 (cf. col. 15, 41-63) must be equal or lower than the avalanche breakdown voltage (cf. col. 16, l. 29-38). *Motivation* to include said teaching by Nagasu et al derives from the undesirability of avalanche breakdown during operation. Furthermore, it would have been obvious to include limitation (b) in view of Chen, who teaches compensation regions 1 (cf. section [0023]) of conductivity type opposite to that of the source region, hence second conductivity type here, disposed below the body zone 4 (cf. section [0023]) "in order to absorb a large part of the electric flux when the layer is fully depleted" (cf. abstract). *Motivation* to include the teaching by Chen in this regard in the invention by Park derives from the possibility to thereby reduce the thickness of the voltage sustaining layer (cf. abstract).

On claim 9: Park uses epitaxial growth techniques to produce region 104 on which the compensation region is formed following Chen, which necessarily must involve the implantation of dopant ions through implantation (cf. col. 5, l. 43-56 in Park). Moreover, the further limitation of claim 9 fails to limit the final structure of the device but instead only limits a method of making of the device.

On claim 10: the compensation regions in the lower part of the device by Chan are at equal altitude, thus allowing the compensation region to be so produced. However, except for the above remark, the further limitation of claim 10 fails to limit the final structure of the device but instead only limits a method of making.

6. ***Claim 6*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Park, Chen and Nagasu et al as applied to claim 1 above, and further in view of Fruth et al (6,011,280). As detailed above, claim 1 is unpatentable over Park in view of Chen and Nagasu et al. Neither Park nor Chen nor Nagasu et al necessarily teach the further limitation defined by claim 6. However, the application of (a) edge termination 34/30 and a (b) channel stop 40 to mitigate the effect of geometrically enhanced edge electric fields through screening provided by dopants and for the purpose of termination the device region, respectively, is well known in the art, as witnessed by Fruth et al (see column 1, line 56 – column 2, line 16).

7. ***Claim 7*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Park, Chen, Nagasu et al and Fruth et al as applied to claim 6 above, and further in view of Feiler (6,236,068 B1). As detailed above, claim 6 (on which claim 7 depends) is unpatentable over Park, Chen, Nagasu et al and Fruth, none of whom necessarily teach the further limitation as defined by claim 7. However, as witnessed by Feiler (cf. Figure 3 and column 6, lines 2-6) it would have been obvious to one of ordinary skill in the art of MOS technology to include the further limitation of claim 7 because source magneto-resistors are thus used to reduce electric field peaks, for example in the vicinity of the gate electrode. The work by Park aims to prevent break-down (cf. col. 1, l. 32-38). In conclusion, there is ample *motivation* to combine the teaching in this regard by Feiler with Park. *Combination* of the teaching by Feiler with the invention by Park is straightforward: the inclusion of a source magneto-resistor can be achieved in a modular fashion, because said magneto-resistor is an additional and modular component extraneous to the substrate. *Success* in implementing the combination can therefore be reasonable expected.

Response to Arguments

8. Applicant's arguments filed 11/25/03 have been fully considered but they are not persuasive. In particular, the amendment of claim 1 introduces new matter

(a) because the compensation component (Figures 4 and 5 and pages has not been disclosed to have a gate insulated from the semiconductor body; instead, Figure 4 clearly shows said gate not to be insulated from said body but instead to abut the latter;

(b) because the compensation component has not been disclosed to have heavily doped terminal regions (corresponding to 9 in Figure 1 or 27 in Figure 5) disposed at the second (i.e., *lower*) main surface, i.e., the surface opposite the gate;

(c) because a further zone of first conductivity (corresponding to zone 10 in Figure 1) disposed in a vicinity of said second main surface has not been disclosed for the compensation component; and

(d) because punch-through regions (such as 12 in Figure 12) disposed between said heavily doped terminal regions have not been disclosed for the compensation component at least for lack of disclosure of said heavily doped terminal regions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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JPM
February 8, 2004